



# PREPARATORY ACTION ON DEFENCE RESEARCH



## **SESSION Electronic Design Technologies for Defence Applications**

INFODAY AND BROKERAGE EVENT  
12 APRIL 2018

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## Call Text presentation RA Topic Call PADR-EDT-02-2018

European high-performance, trustable (re)configurable system-on-a-chip or system-in-package for defence applications

# PADR-EDT-02-2018 - Challenge (1/2)

## Electronic Design Technologies for Defence Applications

- New military requirements: more processing power required
- Need for defence-specific HW & SW approaches:
  - Application Specific Integrated Circuits (ASIC)
  - Programmable Logic Devices (PLD) like Field Programmable Gate Array (FPGA)
  - System-On-Chip (SoC)
  - System-In-Package (SiP)
- Solution should strike a balance between the requirements of the defence applications and economic drivers.

# PADR-EDT-02-2018 - Challenge (2/2)

## Electronic Design Technologies for Defence Applications

Setting up a EU-based supply chain for high-performance, trustable (re)configurable SoC/SiP for defence applications would contribute to:

- Avoid **risks of supply chains and vulnerabilities** in terms of security due to dependence on non-EU suppliers;
- Remove **end-user restrictions** on use of technologies imposed by non-EU nations' regulations;
- Create **business opportunities** in other highly demanding sectors beyond the defence sector.

# PADR-EDT-02-2018 – Scope (1/5)

## Electronic Design Technologies for Defence Applications

Design and validate a SoC/SiP:

- Make a substantial contribution towards the development and manufacturing of **European high-performance, trustable (re)configurable SoC/SiP suitable for multiple defence applications;**
- Take into account **long-term operation under harsh conditions;**
- **Match the production capabilities** of ideally more than one trustable fab or foundry established in the EU;
- Explore advancing **innovative development and debugging tools;**
- Demonstrate **enhanced performance** and shorter development times.

# PADR-EDT-02-2018 – Scope (2/5)

## Electronic Design Technologies for Defence Applications

Security protection of the proposed hardware and software solutions:

- SoC/SiP architecture should be **protected from intrusion or attacks**;
- **Design and manufacturing process should be highly controlled** to exclude that weaknesses, back doors or Trojan horses are implemented in the hardware and software components and systems;
- **Flexible packaging options** should be offered and known good dies (KGD) should be supplied as well when requested;
- Protection measures should be in line with the **recommendations issued by the relevant national crypto approval authorities (CAA)** of at least two Member States or Norway to handle information up to the national equivalents of SECRET UE/EU SECRET.

# PADR-EDT-02-2018 – Scope (3/5)

## Electronic Design Technologies for Defence Applications

Proposals should include:

- **SWaP-C analysis** to support the proposed (re)configurable SoC/SiP technology;
- High-level description of the **key performance indicators** (KPIs) for state-of-the-art performance of the envisaged functionalities;
- **Methodologies** on how to measure them.

# PADR-EDT-02-2018 – Scope (4/5)

## Electronic Design Technologies for Defence Applications

Minimum features:

- Implemented in a **technology node** of 28 nm or smaller;
- If the proposed architecture includes a **FPGA**:
  - 200k Look-Up Table (**LUTs**);
  - Internal **non-volatile memory**;
  - **Digital Signal Processing hard-macros**;
  - **Flexible interconnections** between the DSP processing core, general processing cores and on- and off chip bridges and interfaces;
  - **Encryption module** and anti-tamper and TEMPEST protection;
  - At least 10 Gb/s **high-speed links / interfaces**.



# PADR-EDT-02-2018 – Scope (5/5)

## Electronic Design Technologies for Defence Applications

- When relevant, results publicly available from EDA and NATO activities and studies should be taken into account for the proposed work.
- The implementation of this topic is intended to start at TRL 2 to 3 and target TRL 5.
- EU contribution: EUR 8 000 000 to 12 000 000.
- **No more than one action will be funded.**
- **Deadline for applications: 28/06/2018**

# PADR-EDT-02-2018 – Expected impact

## Electronic Design Technologies for Defence Applications

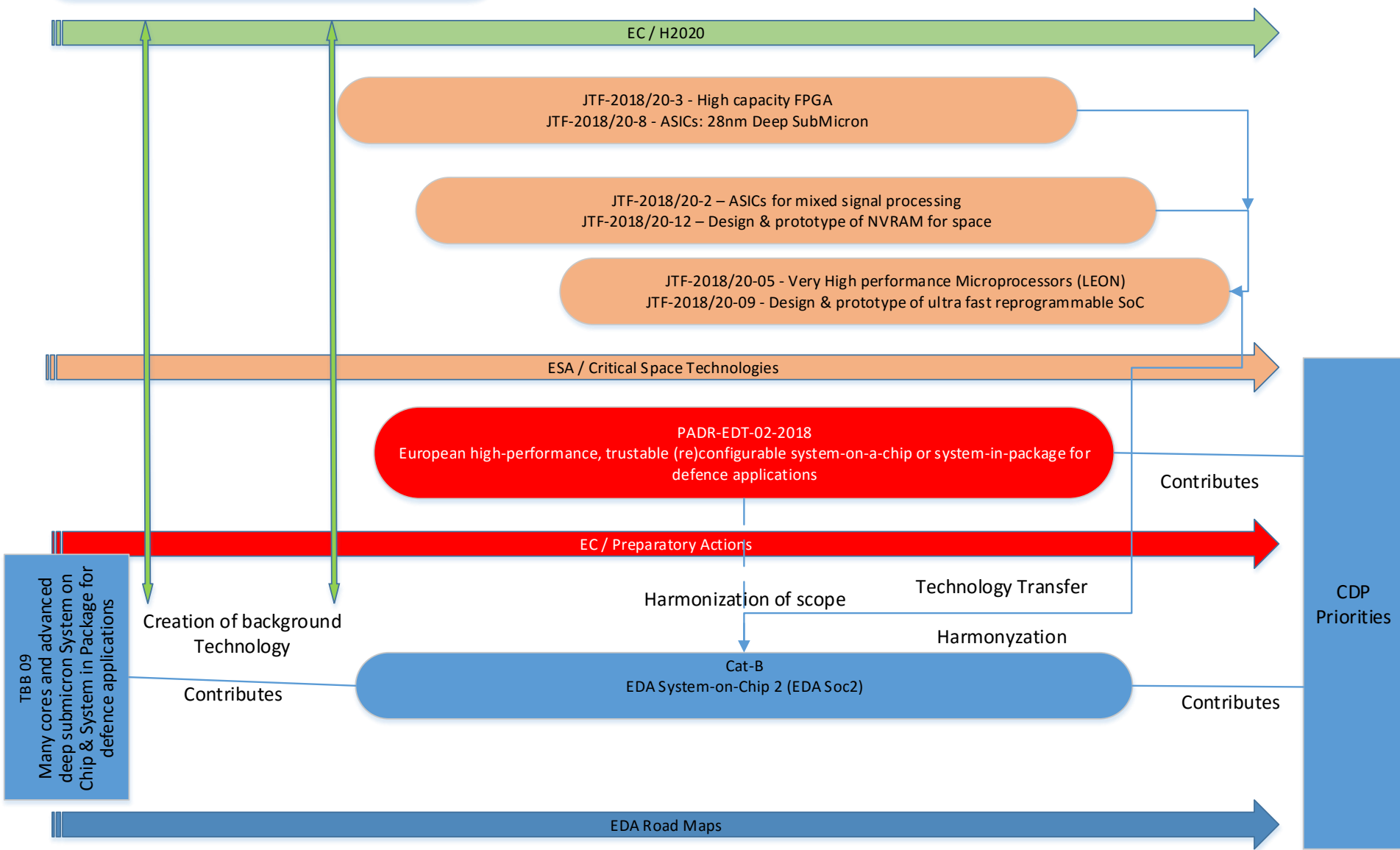
- Convincing demonstration of the potential of EU-funded research in support of EU critical defence technologies,
  - In particular in the domain of (re)configurable SoC/SiPs;
- Ensure secure and autonomous availability of high performance and trustable (re)configurable SoC/SiPs to military end-users;
- Contribute to strengthening the European microelectronics industry and help improve its global position through the implementation of innovative technologies along a new European manufacturing value chain;
- Improved competitiveness of the end-user industry in and beyond the defence sector.

**Type of Action:** Research Action (RA)

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Information on other projects / studies



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## Questions and Answers

## Why is work on Application Specific Integrated Circuits (ASICs) outside the scope of the PADR-EDT-02-2018 call?

### Answer:

Proposals submitted to this call should design and validate a SoC/SiP and as such make a substantial contribution towards the development and manufacturing of European high-performance, trustable (re)configurable SoC/SiP suitable for multiple defence applications.

By definition, ASICs are designed and configured to execute a dedicated (set of) tasks for a specific application, albeit with highly improved performance.

Moreover, their configuration is defined at the level of the design, rather than at the level of the user application.

Both characteristics make ASICs less suited to for the flexibility required in this call topic and hence work on ASICs is deemed to be outside the scope of this call.

However, proposals that include work (design, architectures, ...) that make use of ASICs while keeping the desired level of flexibility specified in the call, could be in scope.

## Could research proposals submitted to the 2018 calls on critical defence technologies (PADR-EDT-02-2018 and PADR-EF-02-2018) include background that is subject to end-user restrictions?

### Answer:

As specified in the impact section of the call text, the aim of these calls is to fund research projects that will generate substantial contributions to ensure secure and autonomous availability of components and systems to military end users.

End-user restrictions on background to be used in the project could severely reduce the impact of the proposal on this point.

The description on the agreement on background (section 3.5 of the technical annex of the proposal template) should carefully cover such restrictions.

The description should in addition propose development of alternatives that could lift such restrictions as part of the project.

# Other Questions?

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Thanks for your attention