EDA-B-1505-IAP1-GP

CRITICAL DIGITAL TECHNOLOGIES FOR DEFENCE: SYSTEM-IN-PACKAGE (SIP) & SYSTEM-ON-CHIP (SOC)

Participating Members

Consortia/Organization

Digitalisation encompasses high performance signal processing for RF sensors, cryptographic processing, data processing and storage for military network and decision-making. It is also a key enabler for the next generation of satellites navigation payloads and Earth observation instruments. The advancing miniaturisation of semiconductor structures is currently the only way to reduce the relative power consumption of logic components while simultaneously increasing their performances.

Objectives

» In Mid-2019, Norway and France launched a joint Cat-B project EDA SoC 2 which focused on **advanced silicon technology and anti-tamper integration** on the **FD SoI 28nm** from ST. Kongsberg is the consortium leader, the budget is ~5M€, the duration 3 years and the contract has been signed in October 2019.

» Following the PADR call 2018, EDA has been selected by the European Commission to do the implementation of the project EXCEED. This project aims at developing a **sustainable European supply chain on advanced Field Programmable Gate Array (FPGAs) for defence based on Fully Depleted Silicon-on-Insulator (FD SoI) 28nm technology**. ST is the consortium leader, the budget is ~12M€, the duration 3 years and the contract has been signed in November 2020. On the long term, it is to establish a source of advanced components to support the European non-dependencies on critical digital technologies for defence and space.

Work Strands

» Following research analysis (state of the art, military needs, and gaps) done via two EDA funded studies, and in continuation with previous work done in the Cat-B project EDA SoC, this project will develop and test new features in the most advanced European digital technology (FD SoI 28nm) and will include new anti-tampers mechanisms.

Way Ahead

» Regarding the implementation recommendations resulting from the CapTech Components workshop in September 2018 and the MoD and Industries reviews in March 2019, three topics have been identified as short / mid-term priorities to develop for a European eco-system:

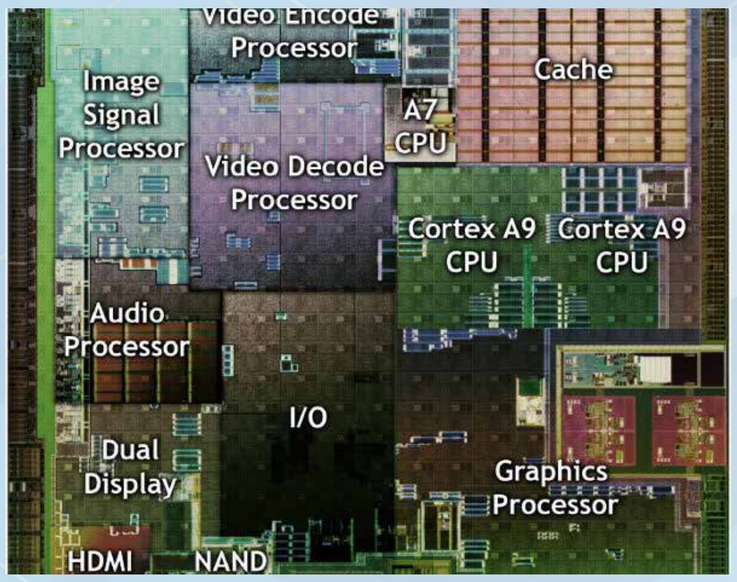
- Extension of the SoC / FPGA family based upon PADR SoC EXCEED,
- Introduction of SiP & Wafer Level Packaging for Digital,
- New and advanced digital processing engines for Defence

European Space Agency and the European Commission H2020 and new Horizon Europe include activities in this field. There are synergies between the various sectors of applications and the strengthening of the industrial base and the supply chain will benefit civil, dual use and defence applications.

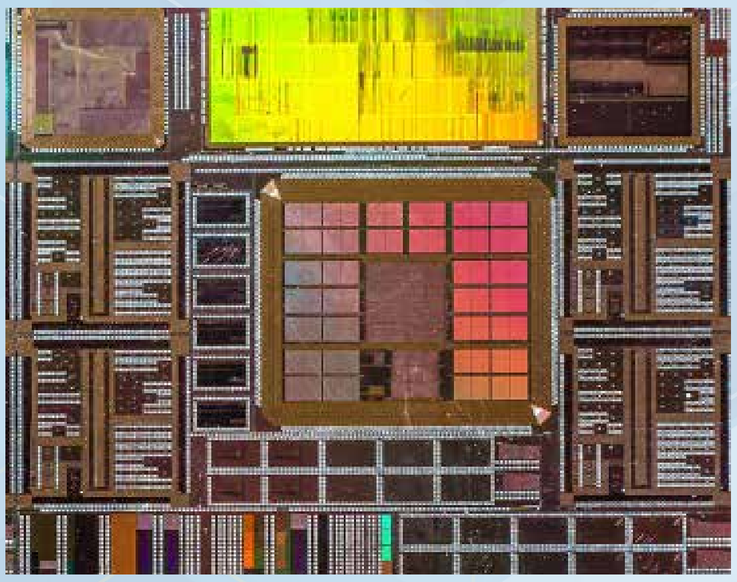
Link to TBBs, other CapTechs, and other links

This activity is supported by work done in CapTech Components, especially related to the SRA update and the following TBBs:

- OSRA TBB43 on system-on-chip,
- OSRA TBB45 on defence critical technology supply chain
- OSRA TBB46 on advanced packaging, PCBs and Thermal management



NVIDIA TEGRA2 chip
(image for illustrative purpose only)



OCTAVO soc
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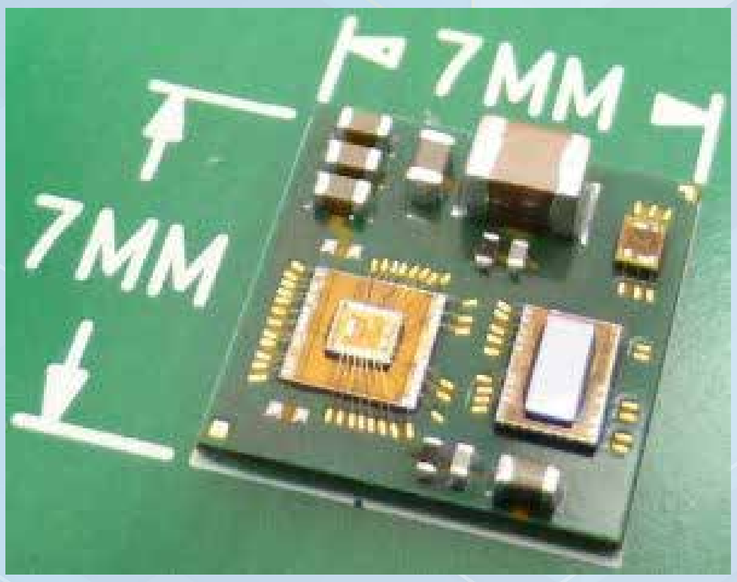

ADI ADAQ400x series
(image for illustrative purpose only)

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